IN THE CLAIMS

1. (Currently Amended) A Pprocess for testing a serializer circuit arrangement ~~where~~comprising:

using the serializer circuit arrangement ~~is used~~ to convert a parallel datastream into a serial datastream by using a multiphase clock signal~~,~~; and

~~wherein~~detecting a phase offset between two clock phases of the multiphase clock signal is detected in order to assess the quality of the multiphase clock signal.

2. (Currently Amended) The Pprocess according to claim 1, wherein to detect the phase offset between the two clock phases corresponding clock phase signals are mixed, a resulting output signal being evaluated to assess the quality of the multiphase clock signal.

3. (Currently Amended) The Pprocess according to claim 2, wherein the output signal resulting from the mixing of the clock phase signals is low pass filtered before being evaluated to assess the quality of the multiphase clock signal.

4. (Currently Amended) The Pprocess according to claim 2, wherein the output signal resulting from the mixing of the clock phase signals is subjected to a voltage/current conversion before being evaluated to assess the quality of the multiphase clock signal.

5. (Currently Amended) The Pprocess for testing a serializer circuit arrangement wherein the serializer circuit arrangement is designed for converting a parallel datastream into a serial datastream by the use of a multiphase clock signal, wherein the ability of the serializer circuit arrangement to transmit a prespecified repetitive digital signal pattern is assessed in that the specified repetitive digital signal pattern is supplied to the serializer circuit arrangement and a

phase offset between a phase of a resulting serial datastream of the serializer circuit arrangement and a clock phase of the multiphase clock signal is detected.

6. (Currently Amended) The ~~P~~process according to claim 5, wherein a prespecified repetitive digital signal pattern comprises a repetitive bit sequence of x bits with a first logic value and x bits with a different second logic value, wherein the phase offset between the serial datastream and a clock phase signal corresponding to the clock phase and divided by a division factor 1/x is detected, with x = 1, 2, 3, ...

7. (Currently Amended) The ~~P~~process according to claim 5, wherein the serial datastream resulting from the prespecified repetitive digital signal pattern of the serializer circuit arrangement is mixed with a clock phase signal corresponding to the clock phase of a multiphase clock signal and the resulting output signal is evaluated.

8. (Currently Amended) The ~~P~~process according to claim 7, wherein the output signal resulting from the mixing of the serial datastream and the clock phase signal is low pass filtered before being evaluated.

9. (Currently Amended) The ~~P~~process according to claim 7, wherein the output signal resulting from the mixing of the serial datastream and the clock phase signal is subjected to a voltage/current conversion before being evaluated.

10. (Currently Amended) The ~~P~~process according to claim 5, wherein the multiphase clock signal has several clock phases with an equidistant phase difference.

11. (Currently Amended) The ~~P~~process according to claim 10, wherein the clock phase signals corresponding to several clock phases of the multiphase clock signal are supplied differentially to the serializer circuit arrangement.

12. (Currently Amended) The ~~P~~process according to claim 5, wherein the multiphase clock signal comprises several clock phase signals of different phase but with the same frequency.

13. (Currently Amended) The ~~P~~process according to claim 5, wherein the several parallel datastreams are supplied to the serializer circuit arrangement in single ended mode while the serial datastream is transmitted differentially.

14. (Currently Amended) The ~~P~~process according to claim 5, wherein the process for testing the serializer circuit arrangement is carried out at wafer level of the serializer circuit arrangement via connections which are not accessible at package level of the serializer circuit arrangement.

15. (Currently Amended) The ~~P~~process according to claim 5, wherein the process for testing the serializer circuit arrangement is carried out via a digital test interface between the serializer circuit arrangement and an external test device to control the test process.

16. (Currently Amended) The ~~P~~process according to claim 5, wherein the process is used to test a serializer circuit arrangement of a high speed communication module.

17. (Currently Amended) A ~~D~~device for testing a serializer circuit arrangement, where the serializer circuit arrangement is designed for converting a parallel datastream into a serial datastream by the use of a multiphase clock signal, the device comprising:

~~wherein~~ phase offset detection means ~~are provided to~~ for detecting a phase offset between two clock phases of the multiphase clock signal~~,~~; and ~~that~~

evaluation means for ~~are provided to~~ evaluate~~ing~~ the phase offset detected by the phase offset detection means in order to assess depending thereon the quality of the multiphase clock signal.

18. (Currently Amended) The ~~D~~device according to claim 17, wherein the phase offset detection means comprise a mixing device for mixing clock phase signals corresponding to the two clock phases, wherein the evaluation means are designed to evaluate an output signal generated by the mixer device as a function thereof.

19. (Currently Amended) The ~~D~~device according to claim 18, wherein the evaluation means comprise a low pass filter device for low pass filtration of the output signal from the mixer device.

20. (Currently Amended) A ~~D~~device according to claim 18, wherein the phase offset detection means comprise a voltage/current conversion device for voltage/current conversion of the output signal of the mixer device.

21. (Currently Amended) A ~~D~~device for testing a serializer circuit arrangement, wherein the serializer circuit arrangement is designed to convert a parallel datastream into a serial datastream by using a multiphase clock signal, wherein evaluation means are provided which are designed such that by supplying a prespecified repetitive digital signal pattern to the serializer circuit arrangement, by evaluating the resulting serial datastream of the serializer circuit arrangement, said means assess the ability of the serializer circuit arrangement to transmit the prespecified repetitive digital signal pattern, and that phase offset detection means are provided to detect a phase offset between a phase of the serial datastream resulting from the prespecified repetitive digital signal pattern of the serializer circuit arrangement and a clock phase of the multiphase clock signal, wherein the evaluation means assess the ability of the serializer circuit arrangement to transmit the prespecified repetitive digital signal pattern by evaluation of the phase offset detected by the phase offset detection means.

22. (Currently Amended) The ~~D~~device according to claim 21, wherein the evaluation means are designed such that they supply to the serializer circuit arrangement the prespecified repetitive

digital signal pattern with a repetitive bit sequence of x bits with a first logic value, and x bits with a different second logic value, wherein a clock phase signal corresponding to a clock phase of the multiphase clock signal is passed via a divisor with a division factor 1/x and the phase offset detection means are designed to detect the phase offset between the phase of the serial datastream of the serializer circuit arrangement and a phase of an output signal output by divisor, with x = 1, 2, 3, ...

23. (Currently Amended) The ~~D~~device according to claim 21, wherein the phase offset detection means comprise a mixing device for mixing a clock phase signal, corresponding to the clock phase of the multiphase clock signal, with the serial datastream, wherein the evaluation means are designed such that they evaluate an output signal generated dependent thereon by the mixer device.

24. (Currently Amended) The ~~D~~device according to claim 23, wherein the phase offset detection means comprise a low pass filter device for low pass filtration of the output signal of the mixer device.

25. (Currently Amended) The ~~D~~device according to claim 23, wherein the phase offset detection means comprise a voltage/current converter device to subject the output signal of the mixer device to a voltage/current conversion.

26. (Currently Amended) A ~~P~~process for testing a deserializer circuit arrangement wherein the deserializer circuit arrangement is designed for converting a serial datastream into a parallel datastream by use of a multiphase clock signal, wherein a phase offset between the two clock phases of the multiphase clock signal is detected in order to assess as a function thereof the quality of the multiphase clock signal.

27. (Currently Amended) The ~~P~~process according to claim 26, wherein the clock phase signals corresponding to the two clock phases are mixed and a resulting output signal is evaluated to assess the quality of the multiphase phase clock signal.

28. (Currently Amended) The ~~P~~process according to claim 27, wherein the output signal resulting from the mixing of the clock phase signals is low pass filtered before being evaluated to assess the quality of the multiphase clock signal.

29. (Currently Amended) The ~~P~~process according to claim 28, wherein the output signal resulting from the mixing of the clock phase signals is subjected to a voltage/current conversion before being evaluated to assess the quality of the multiphase clock signal.

30. (Currently Amended) A ~~P~~process for testing a deserializer circuit arrangement wherein the deserializer circuit arrangement is designed to convert a serial datastream into a parallel datastream, and wherein the deserializer circuit arrangement is designed for clock and data recovery from the serial datastream, wherein to assess the quality of a data eye sampled by the deserializer circuit arrangement for data recovery, a clock phase signal is supplied to the deserializer circuit arrangement as an input signal and is sampled with a constant clock phase of a further clock phase signal which essentially has the same frequency as the clock phase signal supplied as an input signal, wherein the phase of the clock phase signal supplied as the input signal is varied and a resulting transition in a data word obtained by sampling the clock phase signal from a first bit pattern to a second bit pattern is evaluated.

31. (Currently Amended) The ~~P~~process according to claim 30, wherein the clock phase signal, which is supplied to the deserializer circuit arrangement as an input signal for testing the deserializer circuit arrangement, is a clock phase signal of a multiphase clock signal, the further clock phase signal used for sampling being a different further clock phase signal of the multiphase clock signal.

32. (Currently Amended) The ~~P~~process according to claim 31, wherein between the clock phase signal supplied to the deserializer circuit arrangement as an input signal and the clock phase signal used for sampling there is a phase difference of 90°.

33. (Currently Amended) The ~~P~~process according to claim 30, wherein the first bit pattern corresponds to a sequence of bits with alternately a first logic value and a different second logic value, where the second bit pattern corresponds to a bit pattern inverted to the first bit pattern.

34. (Currently Amended) The ~~P~~process according to claim 30, wherein the deserializer circuit arrangement has for data and clock recovery a phase control circuit with a phase detector and a phase interpolator, wherein to test the deserializer circuit arrangement the clock phase signal supplied as an input signal is supplied to the phase detector while the clock phase used for sampling is supplied to the phase detector via the phase interpolator, and wherein the propagation delay of the clock phase signal, supplied as an input signal, to the phase detector essentially corresponds to the propagation delay of the clock phase used for sampling via the phase interpolator to the phase detector.

35. (Currently Amended) The ~~P~~process according to claim 34, wherein to test the quality of the data eye of the deserializer circuit arrangement, operation of the phase control circuit is frozen.

36. (Currently Amended) The ~~P~~process according to claim 30, wherein to assess the quality of the data eye of the deserializer circuit arrangement, a number of different values of the data word, obtained by sampling the clock phase signal supplied as an input signal during the phase change, between the first bit pattern and the second bit pattern are evaluated.

37. (Currently Amended) The ~~P~~process for testing a deserializer circuit arrangement, wherein the deserializer circuit arrangement is designed to convert a serial datastream into a parallel datastream, and wherein the deserializer circuit arrangement is designed for clock and data recovery from the supplied serial datastream, wherein to test the clock recovery of the deserializer circuit arrangement, a clock phase signal is supplied as an input signal to the deserializer circuit arrangement, wherein a clock signal then recovered by the deserializer circuit arrangement from the supplied clock phase signal is compared with the clock phase signal supplied in order to assess as a function thereof the clock recovery of the deserializer circuit arrangement.

38. (Currently Amended) The ~~P~~process according to claim 37, wherein the clock phase signal supplied to test the clock recovery of the deserializer circuit arrangement corresponds to a clock phase of a multiphase clock signal.

39. (Currently Amended) The ~~P~~process according to claim 37, wherein the phase of the clock phase signal supplied as an input signal to the deserializer circuit arrangement changes and the clock signal then recovered therefrom is compared with the supplied clock phase signal with the changed phase in order to assess whether the clock signal recovered by the deserializer circuit arrangement reconstructs the phase change of the supplied clock phase signal.

40. (Currently Amended) The ~~P~~process according to claim 37, characterised in to compare the recovered clock signal with the clock phase signal supplied to test the deserializer circuit arrangement, the clock phase signal supplied is mixed with the recovered clock signal, wherein a resulting output signal is evaluated.

41. (Currently Amended) The ~~P~~process according to claim 40, wherein the output signal resulting from mixing the supplied clock phase signal with the recovered clock signal is low pass filtered before being evaluated.

42. (Currently Amended) The ~~P~~process according to claim 40, wherein the output signal resulting from mixing the supplied clock phase signal with the recovered clock signal is subjected to a voltage/current conversion before being evaluated.

43. (Currently Amended) The ~~P~~process according to claim 37, wherein a multiphase clock signal with several clock phases with equidistant phase difference is supplied to the deserializer circuit arrangement.

44. (Currently Amended) The ~~P~~process according to claim 43, wherein the clock phase signals corresponding to the individual clock phases of the multiphase clock signal are supplied differentially to the deserializer circuit arrangement.

45. (Currently Amended) The ~~P~~process according to claim 43, wherein the multiphase clock signal comprises several clock phase signals with the same frequency but different phase.

46. (Currently Amended) The ~~P~~process according to claim 37, wherein the serial data stream is supplied differentially to the deserializer circuit arrangement while the parallel datastreams are transmitted in single ended mode by the deserializer circuit arrangement.

47. (Currently Amended) The ~~P~~process according to claim 37, wherein the process for testing the deserializer circuit arrangement is carried out at wafer level of the deserializer circuit arrangement via connections which are not accessible at package level of the deserializer circuit arrangement.

48. (Currently Amended) The ~~P~~process according to claim 37, wherein the process for testing the deserializer circuit arrangement is carried out via a digital test interface to an external test device to control the test process.

49. (Currently Amended) The ~~P~~process according to claim 37, wherein the process is used to test a deserializer circuit arrangement of a high speed communication module.

50. (Currently Amended) A ~~D~~device for testing a deserializer circuit arrangement, wherein the deserializer circuit arrangement is designed to convert a serial datastream into a parallel datastream by use of a multiphase clock signal, wherein phase offset detection means are provided to detect a phase offset between two clock phases of the multiphase clock signal, and that evaluation means are provided to assess the quality of the multiphase clock signal by evaluating the phase offset detected by the phase offset detection means.

51. (Currently Amended) The ~~D~~device according to claim 50, wherein the phase offset detection means comprise a mixer device for mixing clock phase signals corresponding to the clock phases, wherein the evaluation means are designed to evaluate an output signal generated by the mixer device.

52. (Currently Amended) The ~~D~~device according to claim 51, wherein the phase offset detection means comprise a low pass filter device for low pass filtration of the output signal generated by the mixer device.

53. (Currently Amended) The ~~D~~device according to claim 51, wherein the phase offset detection means comprise a voltage/current conversion device for voltage/current conversion of the output signal of the mixer device.

54. (Currently Amended) The ~~D~~device for testing a deserializer circuit arrangement, wherein the deserializer circuit arrangement is designed to convert a serial datastream into a parallel datastream, and wherein the deserializer circuit arrangement is designed for clock and data recovery from the serial datastream supplied, wherein evaluation means are provided which are

designed so that to test the quality of a data eye, sampled on data recovery, of the deserializer circuit arrangement said means supply as an input signal a clock phase signal and cause the deserializer circuit arrangement to sample the clock phase signal supplied as an input signal with a constant clock phase of a further clock phase signal, which has essentially the same frequency as the clock phase signal supplied as an input signal, for data recovery from the clock phase signal supplied as the input signal, wherein the evaluation means are designed such that they vary the phase of the clock phase signal supplied as an input signal and evaluate a resulting transition in a data word, obtained on sampling with the constant clock phase, from a first bit pattern to a second bit pattern.

55. (Currently Amended) The ~~D~~device according to claim 54, wherein the clock phase signal supplied as an input signal corresponds to a clock phase of a multiphase clock signal, and that the constant clock phase used for sampling the input signal corresponds to a further clock phase of the multiphase clock signal which differs from the clock phase signal supplied as the input signal.

56. (Currently Amended) The ~~D~~device according to claim 55, wherein the clock phase signal supplied as an input signal and the clock phase used for sampling have a phase difference of 90°.

57. (Currently Amended) The ~~D~~device according to claim 54, wherein the first bit pattern corresponds to a sequence of bits with alternately a first and a different second logic value, wherein the second bit pattern corresponds to the bit pattern inverted to the first.

58. (Currently Amended) The ~~D~~device according to claim 54, wherein digital registers are provided to store the data words obtained by sampling the clock phase signal supplied as an input signal.

59. (Currently Amended) The ~~D~~device according to claim 54, wherein the clock phase signal supplied as an input signal is supplied to the deserializer circuit arrangement via means for changing the phase of this clock phase signal, and that the evaluation means are designed such that they control these means accordingly to vary the phase of the clock phase signal supplied as an input signal.

60. (Currently Amended) The ~~D~~device according to claim 59, wherein the deserializer circuit arrangement has a phase control circuit with a phase detector and a phase interpolator, wherein the clock phase signal supplied as an input signal is supplied to the phase detector via the means for varying the phase of the clock phase signal while the further clock phase signal corresponding to the clock phase used for sampling is supplied to the phase detector via the phase interpolator, and that in a starting state of the device a propagation delay of the clock phase signal used as an input signal to the phase detector via the means for varying the phase essentially corresponds to a propagation delay of the clock phase signal used for sampling to the phase detector via the phase interpolator.

61. (Currently Amended) The ~~D~~device according to claim 60, wherein the evaluation means are designed such that to test the quality of the sampled data eye of the deserializer circuit arrangement, they freeze the operation of the phase control circuit.

62. (Currently Amended) The ~~D~~device according to claim 54, wherein the evaluation means are designed such that to test the quality of the sampled data eye of the deserializer circuit arrangement, they evaluate a number of different values during transition of the data word obtained by sampling the clock phase signal supplied as an input signal from the first bit pattern to the second bit pattern.

63. (Currently Amended) A ~~D~~device for testing a deserializer circuit arrangement, wherein the deserializer circuit arrangement is designed to convert a serial datastream into a parallel

datastream and wherein the deserializer circuit arrangement is designed for clock and data recovery from the serial datastream supplied, wherein evaluation means are provided which are designed such that to test the clock recovery of the deserializer circuit arrangement they supply a clock phase signal as an input signal, and that phase offset detection means are provided to detect a phase offset between the clock phase signal supplied as an input signal and a clock signal then recovered by the deserializer circuit arrangement, where the evaluation means are designed to evaluate the phase offset detected by the phase offset detection means.

64. (Currently Amended) The ~~D~~device according to claim 63, wherein the clock phase signal supplied as an input signal to test the deserializer circuit arrangement corresponds to a clock phase of a multiphase clock signal supplied to the deserializer circuit arrangement.

65. (Currently Amended) The ~~D~~device according to claim 63, wherein the clock phase signal is supplied to the deserializer circuit arrangement via means for varying the phase of the clock phase signal, and that the evaluation means control these means for varying the phase of the clock phase signal and evaluate the phase offset then detected by the phase offset detection means between the clock phase signal with the varied phase and the clock signal recovered by the deserializer circuit arrangement.

66. (Currently Amended) The ~~D~~device according to claim 63, wherein the phase offset detection means have a mixer device for mixing the clock phase signal supplied as input signal with the clock signal then recovered by the deserializer circuit arrangement, where the evaluation means are designed to evaluate an output signal of the mixer device.

67. (Currently Amended) The ~~D~~device according to claim 66, wherein the phase offset detection means comprise a low pass filter device for low pass filtration of the output signal from the mixer device.

68. (Currently Amended) The ~~D~~device according to claim 66, wherein the phase offset detection means comprise a voltage/current conversion device for voltage/current conversion of the output signal from the mixer device.

69. (Currently Amended) The ~~P~~process according to claim 1, wherein the multiphase clock signal has several clock phases with an equidistant phase difference.

70. (Currently Amended) The ~~P~~process according to claim 1, wherein the multiphase clock signal comprises several clock phase signals of different phase but with the same frequency.

71. (Currently Amended) The ~~P~~process according to claim 1, wherein the several parallel datastreams are supplied to the serializer circuit arrangement in single ended mode while the serial datastream is transmitted differentially.

72. (Currently Amended) The ~~P~~process according to claim 1, wherein the process for testing the serializer circuit arrangement is carried out at wafer level of the serializer circuit arrangement via connections which are not accessible at package level of the serializer circuit arrangement.

73. (Currently Amended) The ~~P~~process according to claim 1, wherein the process for testing the serializer circuit arrangement is carried out via a digital test interface between the serializer circuit arrangement and an external test device to control the test process.

74. (Currently Amended) The ~~P~~process according to claim 1, wherein the process is used to test a serializer circuit arrangement of a high speed communication module.

75. (Currently Amended) The ~~P~~process according to claim 27, wherein the output signal resulting from the mixing of the clock phase signals is subjected to a voltage/current conversion before being evaluated to assess the quality of the multiphase clock signal.

76. (Currently Amended) The ~~P~~process according to claim 30, wherein a multiphase clock signal with several clock phases with equidistant phase difference is supplied to the deserializer circuit arrangement.

77. (Currently Amended) The ~~P~~process according to claim 26, wherein a multiphase clock signal with several clock phases with equidistant phase difference is supplied to the deserializer circuit arrangement.

78. (Currently Amended) The ~~P~~process according to claim 30, wherein the serial data stream is supplied differentially to the deserializer circuit arrangement while the parallel datastreams are transmitted in single ended mode by the deserializer circuit arrangement.

79. (Currently Amended) The ~~P~~process according to claim 30, wherein the process for testing the deserializer circuit arrangement is carried out at wafer level of the deserializer circuit arrangement via connections which are not accessible at package level of the deserializer circuit arrangement.

80. (Currently Amended) The ~~P~~process according to claim 30, wherein the process for testing the deserializer circuit arrangement is carried out via a digital test interface to an external test device to control the test process.

81. (Currently Amended) The ~~P~~process according to claim 30, wherein the process is used to test a deserializer circuit arrangement of a high speed communication module.

82. (Currently Amended) The ~~P~~process according to claim 26, wherein the serial data stream is supplied differentially to the deserializer circuit arrangement while the parallel datastreams are transmitted in single ended mode by the deserializer circuit arrangement.

83. (Currently Amended) The ~~P~~process according to claim 26, wherein the process for testing the deserializer circuit arrangement is carried out at wafer level of the deserializer circuit arrangement via connections which are not accessible at package level of the deserializer circuit arrangement.

84. (Currently Amended) The ~~P~~process according to claim 26, wherein the process for testing the deserializer circuit arrangement is carried out via a digital test interface to an external test device to control the test process.

85. (Currently Amended) The ~~P~~process according to claim 26, wherein the process is used to test a deserializer circuit arrangement of a high speed communication module.